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EXAMINER	
SURYAWANSHI, SURESH	
ART UNIT	**PAPER NUMBER**
2115	27

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/477,034	Applicant(s) DOVER ET AL.	
	Examiner Suresh K Suryawanshi	Art Unit 2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/29/04 Pre Amendment*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *48-53 and 56-76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *48-53 and 56-76* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 48-53 and 56-76 are presented for examination.

Claim Objections

2. Claim 48 is objected to because of the following informalities: at line 5, "a second component of a monotonic count" should have been "a second component of the monotonic count" as there is only one monotonic count. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 48-53 and 56-76 are rejected under 35 U.S.C. 102(b) as being anticipated by Okada et al (JP 05290334 A).

5. As per claim 48, Okada et al teach

maintaining a first value for a first counter based on a content of a volatile memory as a first component of a monotonic count [abstract; para 0011; para 0013; para 0035; first memory means; drawing1; RAM];

maintaining a second value for a second counter based on a content of a non-volatile memory as a second component of a monotonic count [abstract; para 0011; para 0013; para 0035; second memory means; drawing1; EEPROM]; and

controlling updates to the first value for the first counter and to the second value for the second counter at control logic by updating the first value for the first counter in response to the reading of the monotonic count [inherent to the system as to display the reading, the system has to read the monotonic count in between the first update and next update of the first counter and thus the first value of the counter is updated in response to the reading of the monotonic count].

6. As per claims 49, 60, 71 and 75, Okada et al teach that the controlling comprises updating the second value for the second counter when the first value for the first counter meets a predetermined condition [abstract; para 011; para 0013; para 0032; para 0035; carry in the low order digit].

7. As per claims 50 and 59, Okada et al teach that wherein controlling updates further comprises disabling read access to the first counter and the second counter while the monotonic count is updated [inherent in the system as during the update process of the monotonic count, the system will disable read access to the first counter and the second counter as both counter make the monotonic counter in order to provide an accurate reading].

8. As per claims 51, 61, 72 and 76, Okada et al teach that wherein the controlling comprises updating the second value upon a power on reset [inherent to the system as to maintain the current up to date value].

9. As per claims 52, 62, 65 and 68, Okada et al teach that wherein the controlling comprises updating the second value by programming a bit location or location in a flash memory [diagram1; EEPROM].

10. As per claim 53, Okada et al teach that wherein the controlling comprises updating the second value by updating a portion of a flash memory when another portion of the flash memory meets a predetermined condition [diagram1; EEPROM, CN2, CN4; para 0019].

11. As per claim 56, Okada et al teach

powering on a monotonic counter, the monotonic counter at least partially basing a count value on a content of a volatile memory utilized for lesser significant bits of the count value and a non-volatile memory utilized for higher significant bits of the count value [abstract; para 0011; para 0013; para 0035; first memory means; drawing1; RAM; second memory means; EEPROM]; and

updating the count value for the monotonic counter by a first value on the powering on condition [inherent to the system as to maintain the current up to date value].

12. As per claim 57, Okada et al teach that wherein the updating the count value for the monotonic counter comprises updating a flash memory to update the non-volatile memory [inherent as a flash memory is a type of non-volatile memory; abstract].

13. As per claim 58, Okada et al teach that

a volatile counter to maintain lesser significant bits of a monotonic count [abstract; para 0011; para 0013; para 0035; first memory means; drawing1; RAM];

a non-volatile counter to maintain higher significant bits of the monotonic count based on a content of a non-volatile memory [abstract; para 0011; para 0013; para 0035; second memory means; drawing1; EEPROM]; and

control logic to control updating the first and second counters by updating the first counter when the monotonic count is read [inherent to the system as to display the reading, the system has to read the monotonic count in between the first update and next update of the first counter and thus the first value of the counter is updated in response to the reading of the monotonic count].

14. As per claim 63, Okada et al teach that wherein the non-volatile memory is separated into more than one block of flash memory, wherein individual blocks of flash memory are arranged to provide cascading of selective number of the higher significant bits of the monotonic count [diagram1; element 8; CN2 and CN4].

15. As per claim 64, Okada et al teach

a volatile memory to maintain a first value for lesser significant bits of a count value for a first counter [abstract; para 0011; para 0013; para 0035; first memory means; drawing1; RAM];

a non-volatile memory to maintain a second value for higher significant bits of the count value for a second counter [abstract; para 0011; para 0013; para 0035; second memory means; drawing1; EEPROM]; and

circuitry to maintain a monotonic count value and to update the count value by a number in response to a read of the count value for the monotonic counter [inherent to the system as to display the reading, the system has to read the monotonic count in between the first update and next update of the first counter and thus the first value of the counter is updated in response to the reading of the monotonic count].

16. As per claims 66 and 69, Okada et al teach that wherein the non-volatile memory comprises a flash memory and wherein the circuitry updates the count value by the number by programming a bit location in the flash memory [diagram1; EEPROM].

17. As per claim 67, Okada et al teach

a volatile memory to maintain a first value for a first counter [abstract; para 0011; para 0013; para 0035; first memory means; drawing1; RAM];

a non-volatile memory to maintain a second value for a second counter [abstract; para 0011; para 0013; para 0035; second memory means; drawing1; EEPROM]; and

circuitry to maintain a count value for a monotonic counter, the circuitry to base the count value at least partially on the first value for lesser significant bits of the count value and the second value for higher significant bits of the count value [abstract; para 0011; para 0013; para 0035; first memory means; drawing1; RAM; second memory means; EEPROM], and to update the count value by a number in response to a powering on condition for the circuitry [inherent to the system as to maintain the current up to date value].

18. As per claim 70, Okada et al teach

one or more registers to store a first value [abstract; para 0011; para 0013; para 0035; first memory means; drawing1; RAM; volatile memory];

a first adder to maintain the first value [inherent in the system as incrementing the count];

a flash memory to store a portion of bits used for a monotonic count [abstract; para 0011; para 0013; para 0035; second memory means; drawing1; EEPROM; non-volatile memory];

one or more registers to store a second value [diagram1; CN2; CN4];

a second adder to maintain the second value based on the one or more programmed locations in the flash memory [inherent in the system as incrementing the count; diagram1; CN2; CN4]; and

a control engine to control the flash memory and the first and second adders, the first value used to determine lower significant bits of the monotonic count and the second value used to determine higher significant bits of the monotonic count, the lesser significant bits being volatile while higher significant bits being non-volatile [abstract; para 0011; para 0013; para 0035; first memory means; drawing1; RAM; second memory means; EEPROM].

19. As per claim 73, Okada et al teach

a monotonic counter comprising:

a volatile counter to maintain a first value [abstract; para 0011; para 0013; para 0035; first memory means; drawing1; RAM; volatile memory];

a non-volatile counter to maintain a second value based on a content of a non-volatile memory [abstract; para 0011; para 0013; para 0035; second memory means; drawing1; EEPROM; non-volatile memory]; and

control logic to control updating the first and second values to control a monotonic count, the volatile counter to generate lesser significant bits of the monotonic count and the non-volatile counter to generate higher significant bits of the monotonic

count [abstract; para 0011; para 0013; para 0035; first memory means; drawing1; RAM; second memory means; EEPROM]; and

one or more processors to read the first and second values [diagram1; CPU; detail description in paras 0020-0027].

20. As per claim 74, Okada et al teach that wherein the control logic controls the volatile counter to update the first value when the first and second values are read [inherent to the system as to display the reading, the system has to read the monotonic count in between the first update and next update of the first counter and thus the first value of the counter is updated in response to the reading of the monotonic count].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K Suryawanshi whose telephone number is 703-305-3990. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
May 25, 2004

Dennis M. Butler
Dennis M. Butler
Primary Examiner